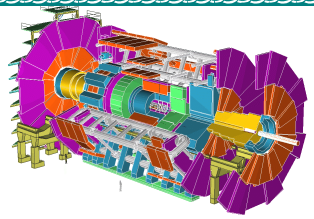
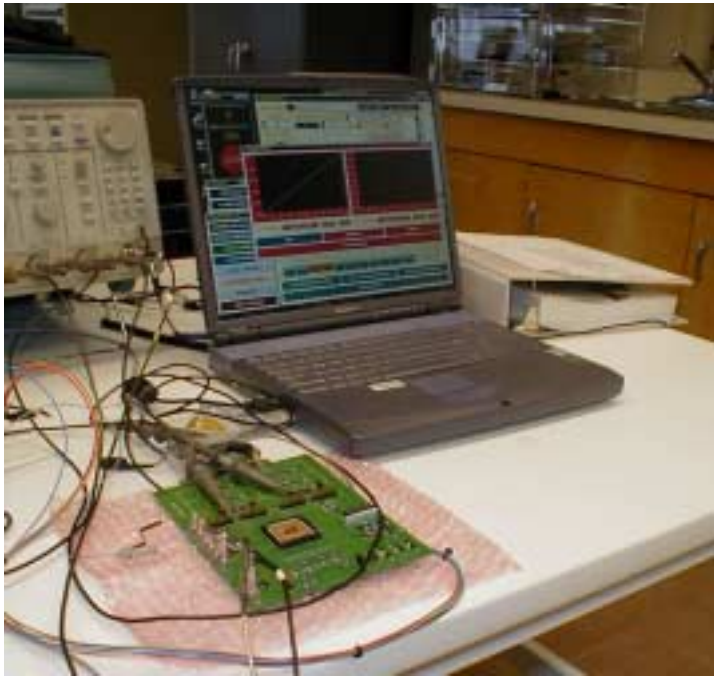


Preliminary Testing of the TSMC Analogue Test Chip @ LBL



FE-I Design Review, CERN, 6th / 7th June 2001

John Richardson
Lawrence Berkeley National Laboratory

Overview

- The LBL Test Set-up
- Irradiation at the 88” Cyclotron
- Global 8-bit DAC Characterisation
- Reference Current
- Front-End Calibration
- Noise and Threshold Perfomance
- TrimDAC Verification
- LVDS Driver & Receiver
- Test Pixel Output Buffer
- TOT Performance
- Timewalk

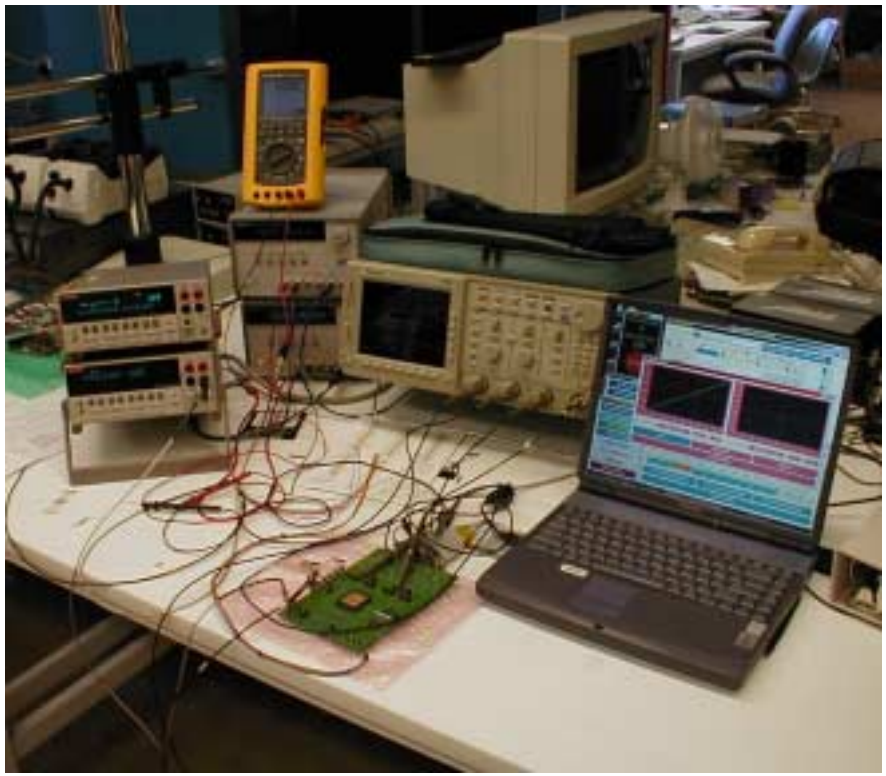
The LBL Test Set-Up

Basis is 32-bit PCMCIA DAQ cardfrom NI (~100 KSamples/s) which is addressable using LabWindows/CVI development environment.

Allows for maximal portability which has proven very convenient for online testing during irradiation e.g.

Interface to lab instrumentation is via USB-GPIB converter.

Test PCB incorparates a direct interface to the DAQ card with level shifters (Philips 74ALVC164245) to convert to/from TTL to CMOS at the ATC digital supply voltage (usually 2.0V).



Also includes a set of AGD728/9 muxes to enable the user to select which DC output (e.g. from the global DACs) to monitor (via a lemo connection). There are also lemo connections used to monitor the test pixel buffer output, to test the LVDS driver/receiver and to provide external calibration pulses.

Irradiation at the 88" Cyclotron

The 88" irradiation facility provides 55MeV protons at a rate of up to ~10^{14} per hour, (can go higher but lose accurate counting ability).

For ionising damage this corresonds to a fluence of 16Mrad, so 50Mrad can be achieved in around 3 hours.

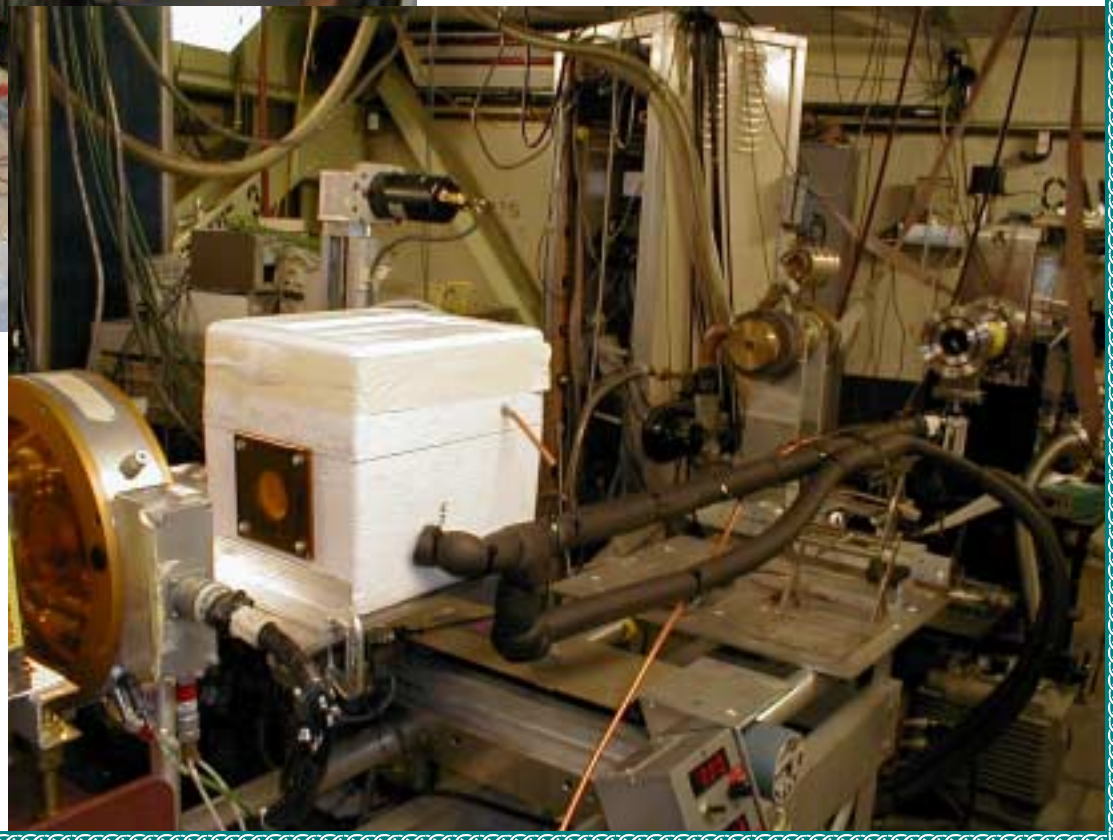
For cooling, a chiller is used to pump a 50/50 mixture of CH_3OH and water through a heat exchanger which is mounted close to a polystyrene cooling box used to contain the DUT .

N2 is just passed through the exchanger and into the box. The distance from the exit of the exchanger to the box is ~15cm thus the temperature of the gas passing through the box tracks the coolant temperature very closely.

A single TSMC analogue test chip was irradiated to a total fluence of 61MRad on May 26th. Continuous testing was performed during the exposure which started off at a relatively low rate and was gradually ramped up.

Periodic checks were made for SEUs in the DAC register, correct operation of one of the global DACs, threshold and noise in a single pixel, the reference current value and the test pixel preamplifier response.

Very minimal analogical changes were observed right up to 61Mrads. SEU bit flips were observed but suspected to be occuring in the shift register itself. Even there the rate corresponded to just ~1 per bit per ATLAS lifetime.

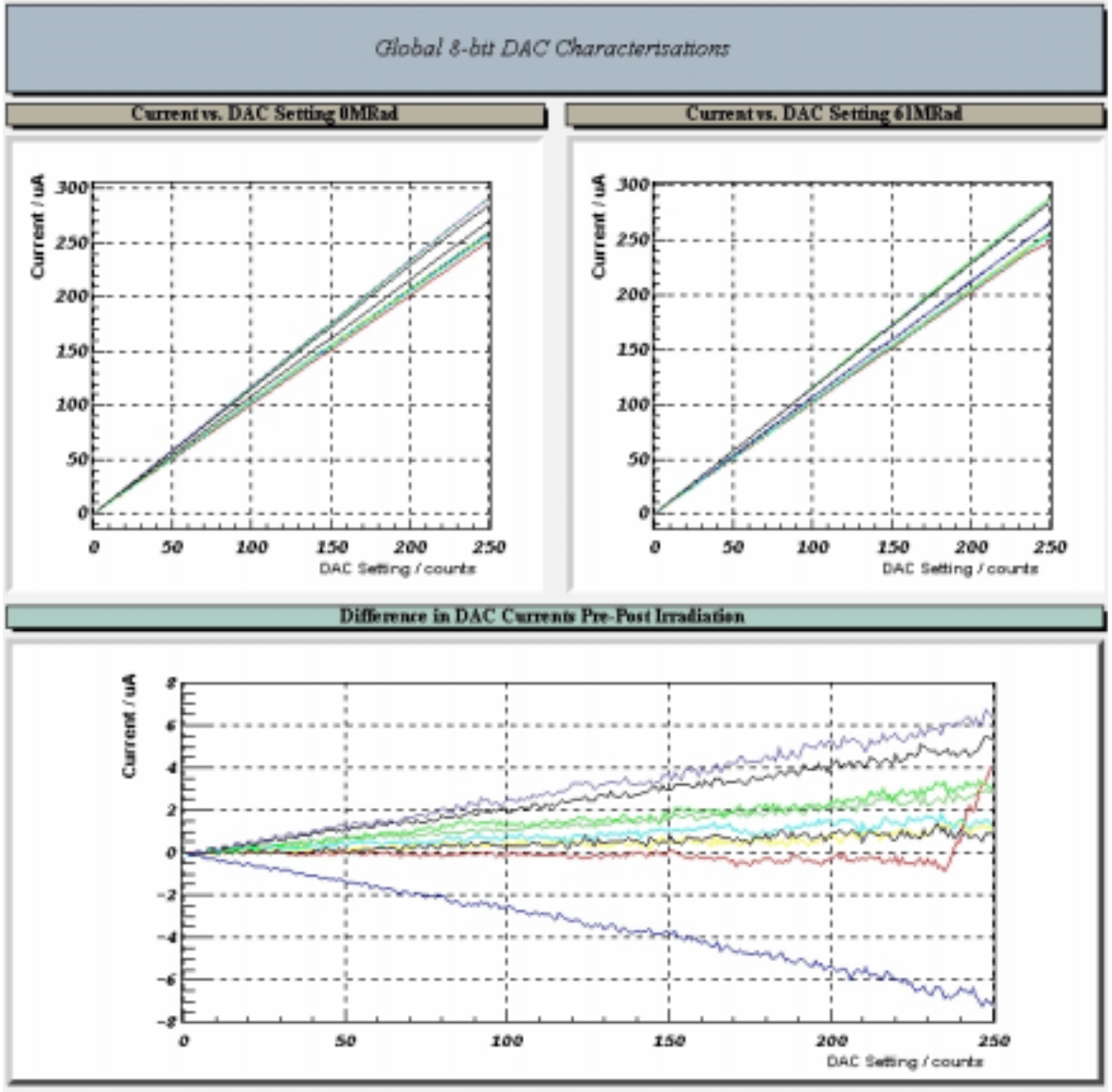


Global 8-Bit DAC Characterisation

All DACs bar VCAL exhibit very linear behaviour. Variation on this chip ~15%.

These plots show the measured current vs. DAC setting before and after 61MRad irradiation.

Typically the change induced by radiation is of the order of 2%.

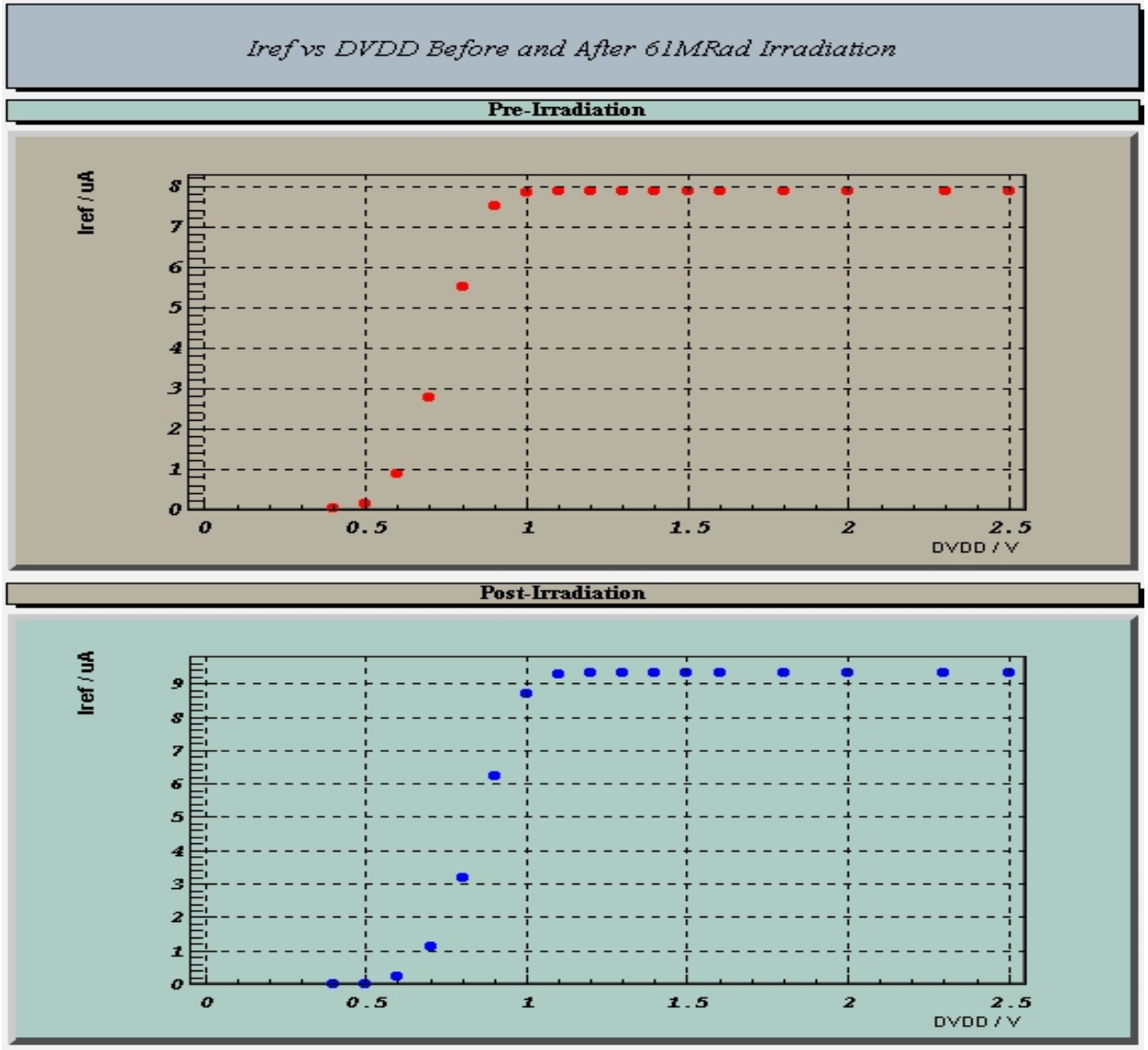


Reference Current

These plots show the reference current versus the applied supply voltage before and after 61MRad.

The turn-on voltage hardly changes at all. Operates at just over 1V after irradiation.

A slight increase in the plateau is observed which is ~3%.



Front-End Calibration

Two injection capacitances available (C_{inj}-hi & C_{inj}-lo), need to determine their magnitudes. Need also to calibrate the VCAL DAC.

The VCAL DAC calibration may be determined in 3 ways:

- **Direct measurement of the DAC voltage vs. setting**
- **Comparison of threshold measurements with external charge injection**
- **Comparison of the test-pixel preamplifier pulse amplitude with external injection**

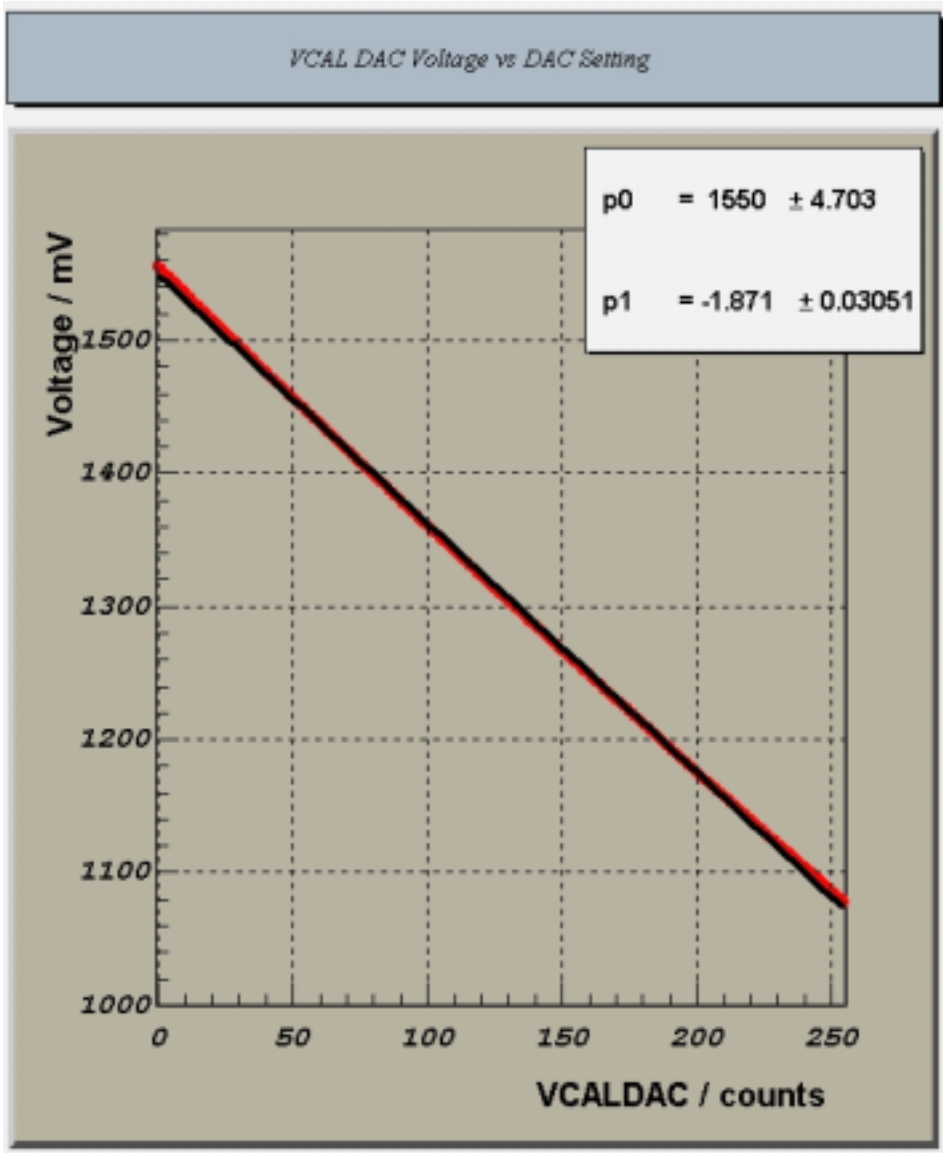
These measurements may be used to determine the magnitude of the VCAL step (per DAC count), the ratio of C_{inj}-hi:C_{inj}-lo and the presence of offsets arising from the chopper or the VCAL DAC.

The test-pixel preamplifier buffered-output may then be used to deduce the feedback capacitance C_f by measuring the gradient of the pulse recovery period (correcting for the gain of the buffer) and the feedback current I_f.

Once C_f is known, C_{inj} may be deduced by determining the gain of the preamp, (again using the test pixel buffer).

Direct measurement of the VCAL DAC voltage indicates an offset of ~45mV at VCALDAC=0. This is now known to be due to a voltage drop across the DAC power supply trace (10Ω resistance).

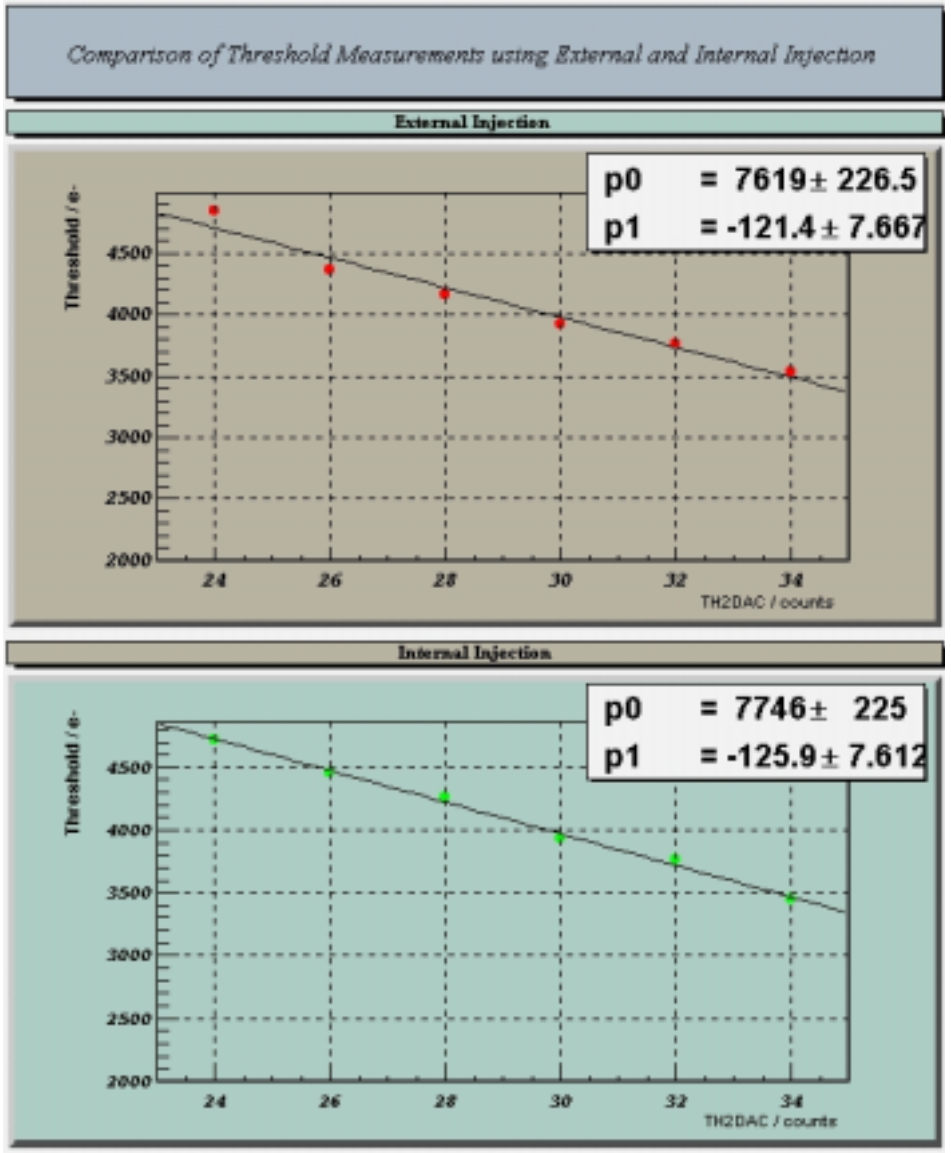
The plot shows a nonlinearity also which shows up as a departure of the data (red) from a straight line fit (black) at the low end and the high end, (c.f. Peter's talk).



Direct comparison of threshold measurements performed using internal and external injection surprisingly show very good agreement in scale and offset (here I am scanning the threshold DAC and assuming 2.5fF for the low injection capacitance).

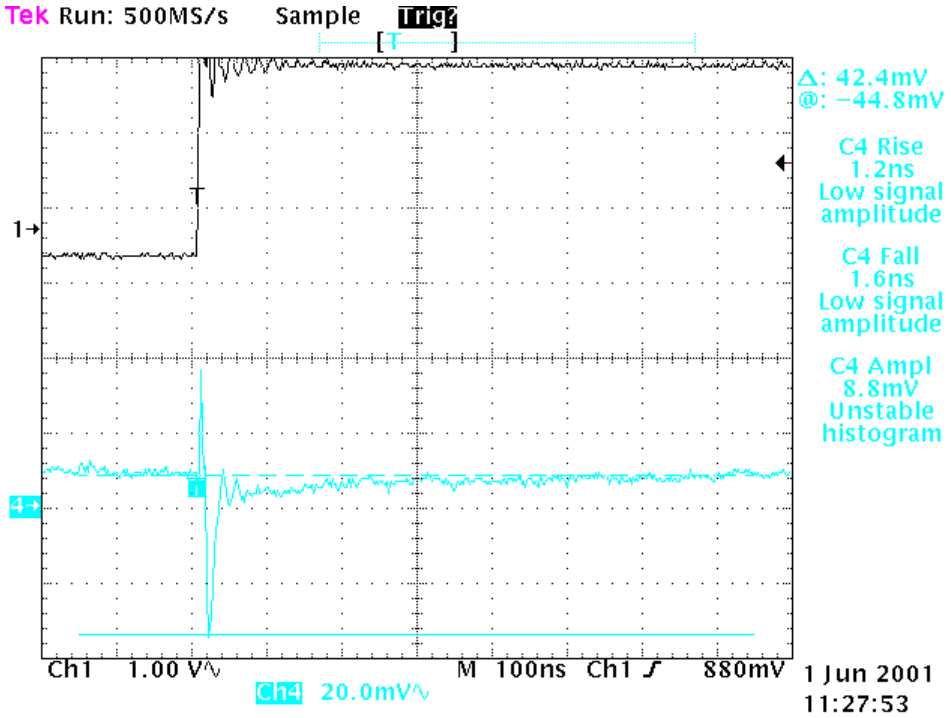
Expect an difference of ~680e- due to the VCAL voltage offset. The offsets between the plots on the right are inconsistent with this.

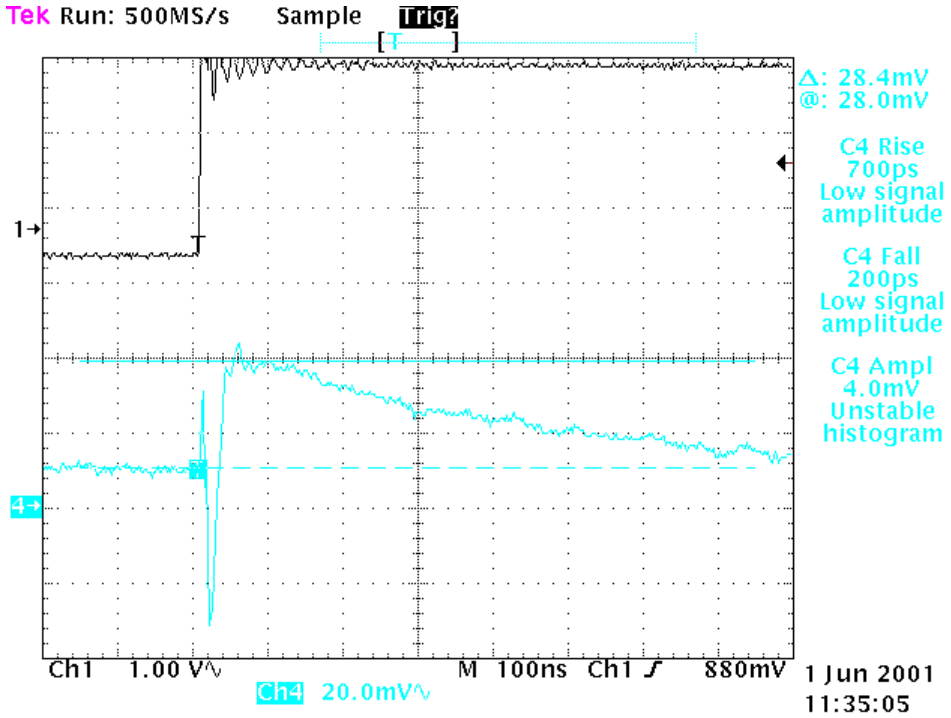
Suspect that there may be an offset induced by the internal chopper circuit which compensates the VCAL offset.



Investigation of the test pixel preamplifier buffered output pulse in internal injection mode for VCAL=0 clearly indicates the DAC offset in high capacitance mode (right). For low capacitance mode however (left) the trace is dominated by a negative going spike which is always be present when the chopper is in use.

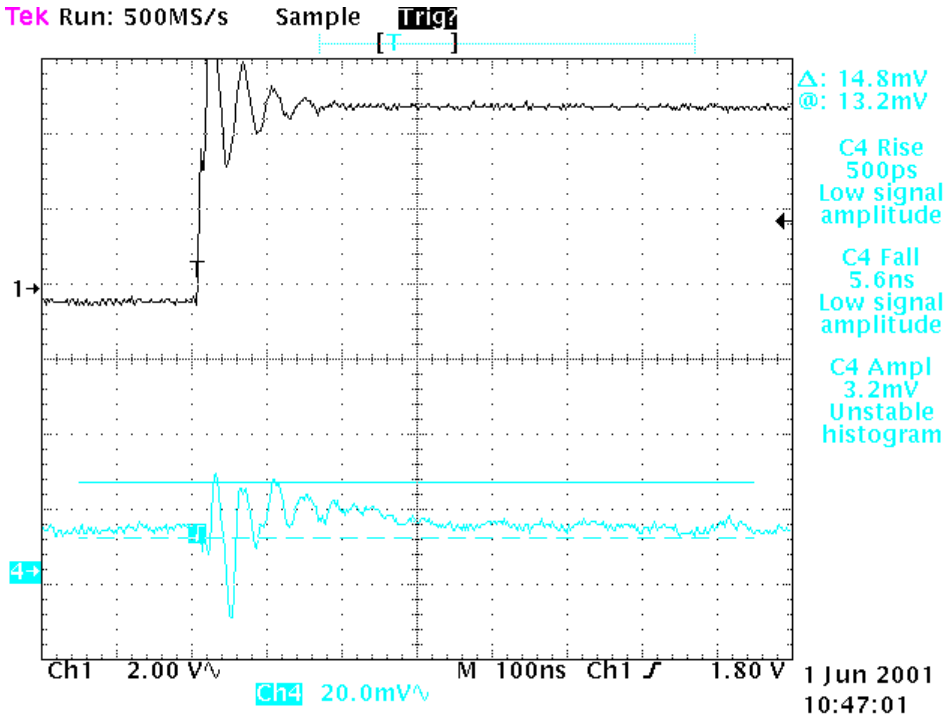
The magnitude of this spike is independent of the voltage-step and whether the small or large calibration capacitor is used.

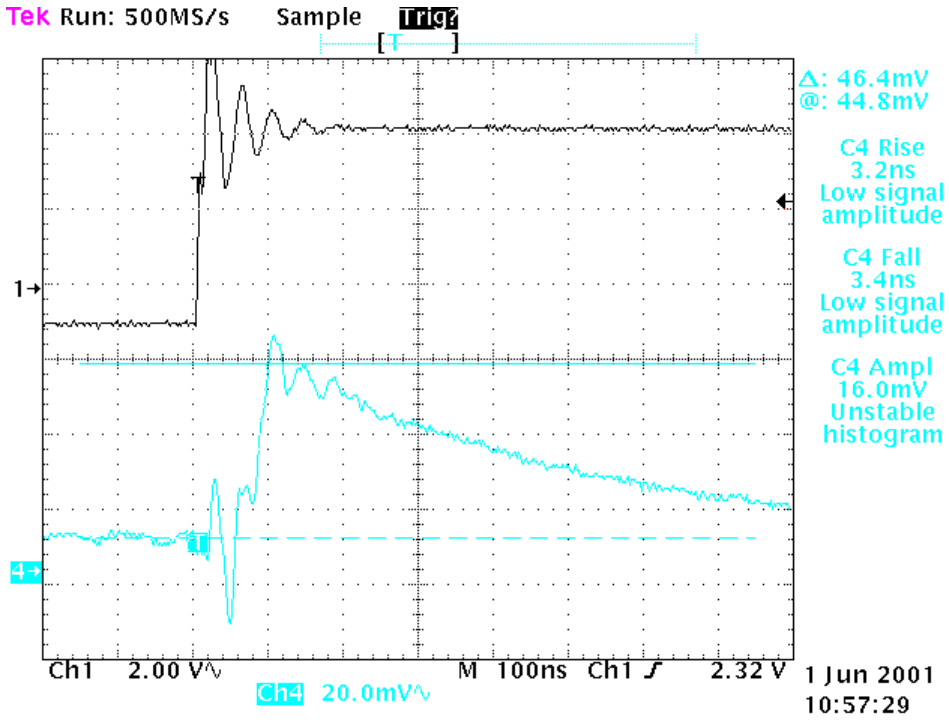


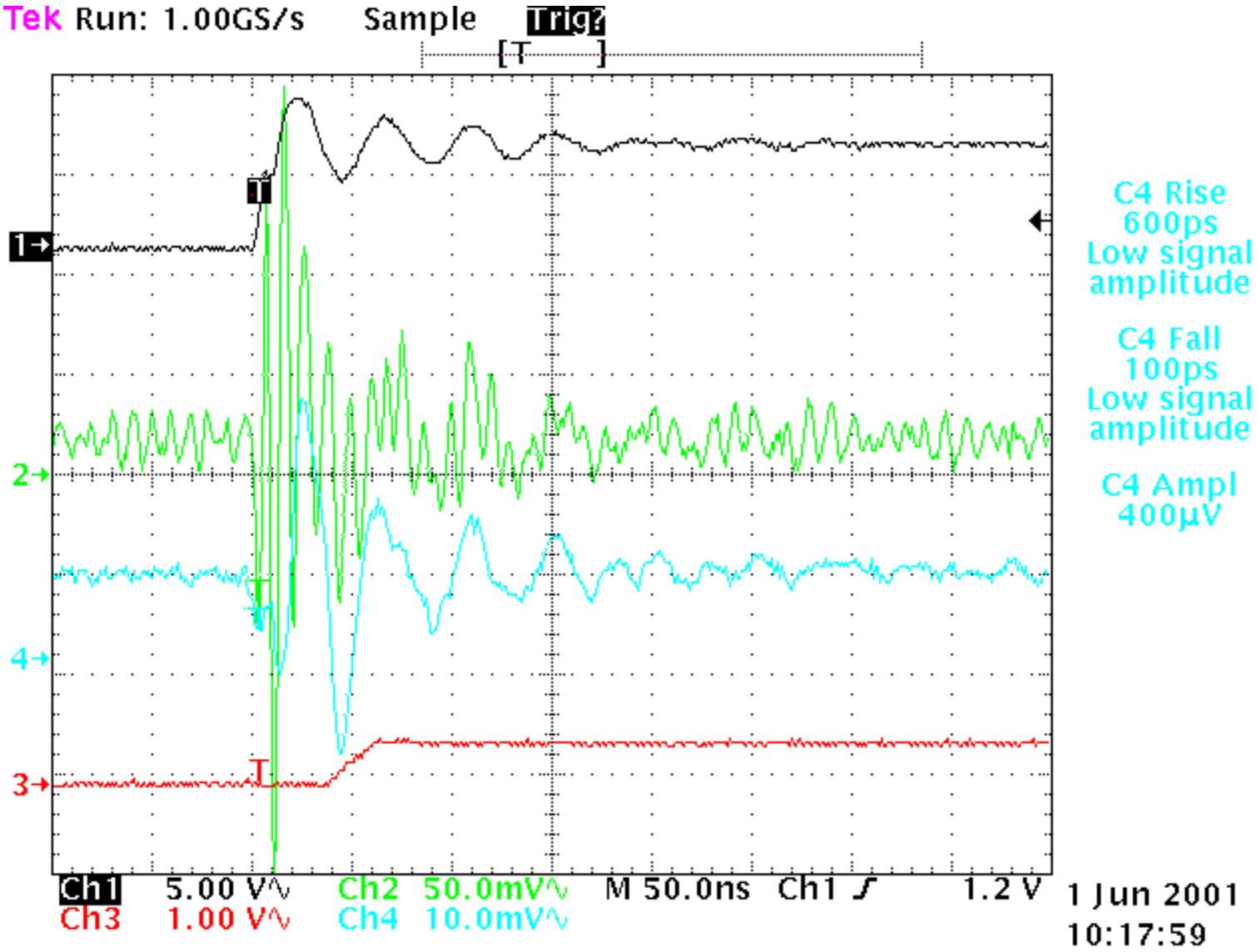


In external injection mode the preamp pulse has a brief ringing phenomenon at the start of the rising edge. This is present even when the pulse isn't injected into the pixel (but the trigger is present on the DAQ bus). Ringing may also be seen on the trigger itself here (scope channel 1).

Further investigation is required to understand this problem. Here I am injecting 50mV in low-capacitance mode (left) and high-C mode (right).





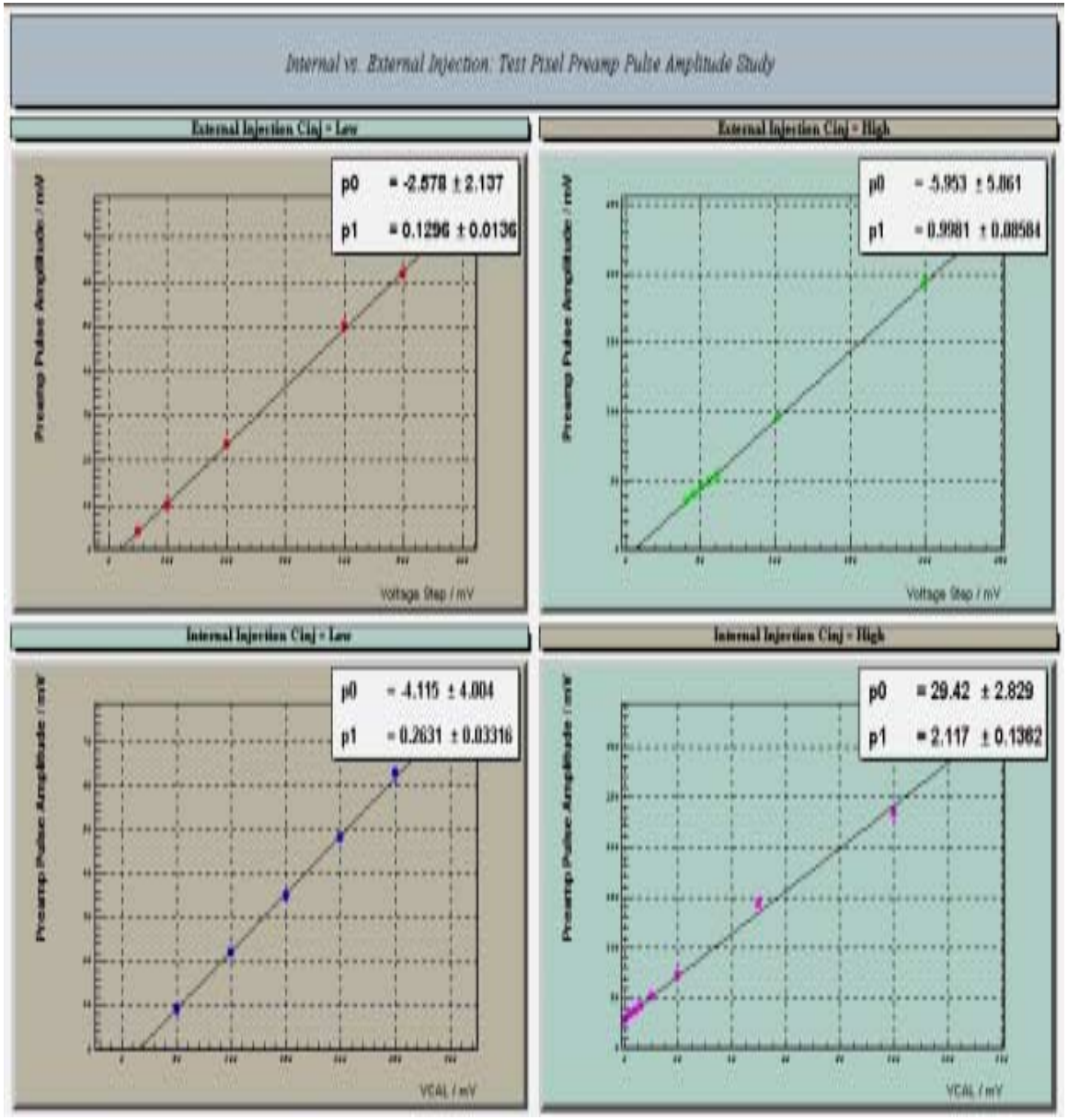

Tek Run: 1.00GS/s Sample Trig?
C4 Rise
600ps
Low signal
amplitude
C4 Fall
100ps
Low signal
amplitude
C4 Ampl
400µV
Ch1 5.00 V
Ch2 50.0mV
M 50.0ns Ch1 1.2 V
Ch3 1.00 V
Ch4 10.0mV
1 Jun 2001
10:17:59

Here the preamplifier pulse height measured on the scope is measured as a function of input voltage step size for external injection (top) and internal injection (bottom) using the low capacitance injection mode (left) and the high-C mode (right).

Deduce using the external mode that the ratio of injection capacitances (given by the ratio of gradients) is 1.00/0.13 = 7.7.

In external mode the offsets are consistent with zero. In internal-low mode the offset is also consistent with zero (which itself is consistent with the threshold measurement result).

In internal high mode the offset is measured to be 29.4+/-2.8mV (on the input side).



The feedback capacitance was estimated using the preamp recovery gradient for a known feedback current (measured accurately using the leakage current measure feature (see later)).

For a feedback current of 1.13nA the gradient was measured to be 27.6mV/282ns (buffered). Correcting for the buffer gain (0.63) and allowing for the fact that the feedback capacitor is discharged by 2 X I_f :

$$C_f = I_f\, dt/dV = (0.63 * 2 * 1.13e\text{-}9 * 282e\text{-}9) / 27.6e\text{-}3 = 14.55fF$$

Applying the measured preamp gain from the external injection (with low C_{inj}) study (correcting for the buffer gain) gives an estimate for the low injection capacitance:

$$C_{inj}\text{-lo} = \text{preamp gain} * C_f = 0.166 * 14.55e\text{-}15 = 2.42fF$$

Also since C_{inj}-hi / C_{inj}-lo is estimated to be 7.7 I deduce:

$$C_{inj}\text{-hi} = 7.7 * C_{inj}\text{-lo} = 18.6fF$$

The extracted values for C_{inj}-lo, C_{inj}-hi and C_f were 2.5, 24.0 and 11.1fF respectively

Threshold and Noise Performance

Measurements of noise using this set-up have proven somewhat tricky as there is a clear susceptibility to pickup from e.g. lab instruments.

Initially measured 300e- before this was realised. Have now made noise measurements as low as 140e-. More usually the number is in the range 180-220e- (with no applied load or injected leakage current). The values wander around from scan to scan.

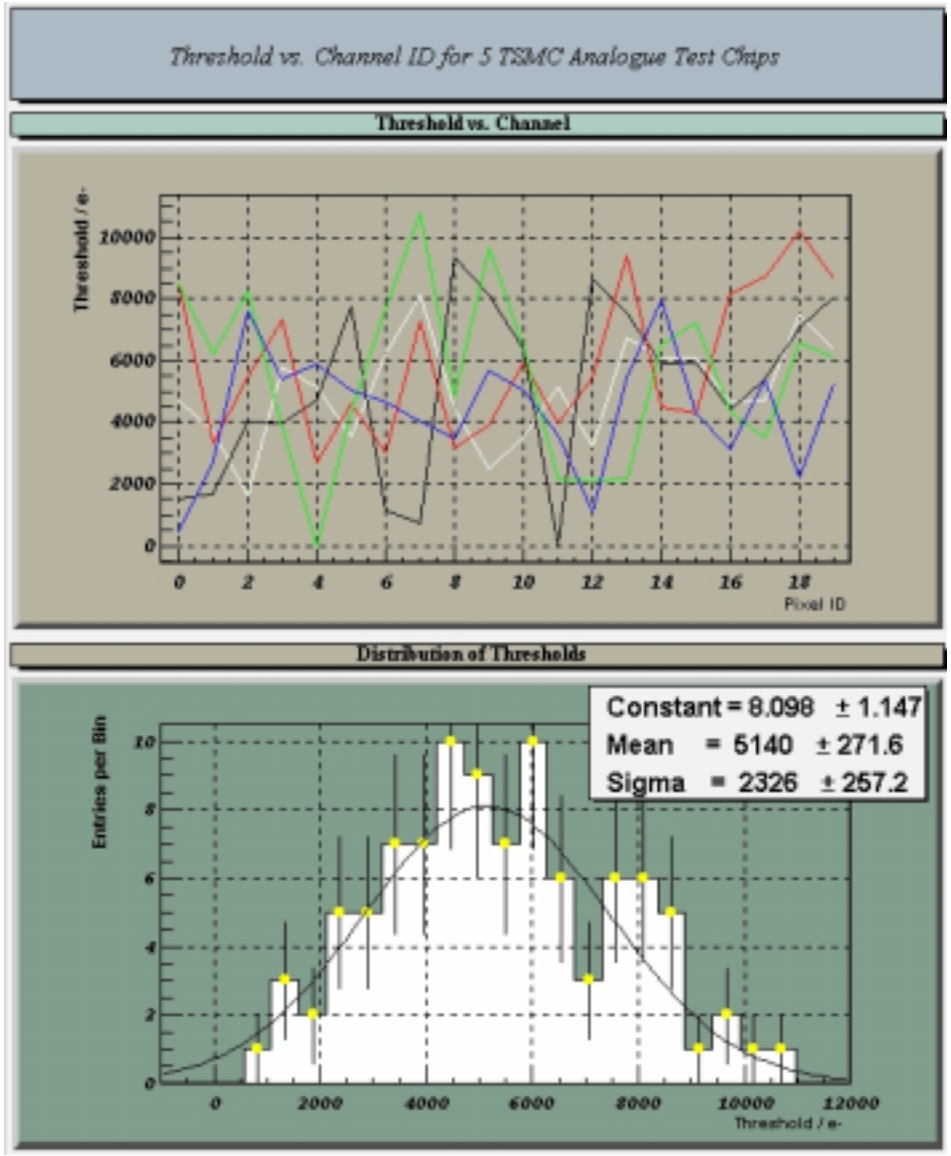
As far as threshold measurements are concerned the overwhelming observation from our test set-up is a very large channel to channel dispersion. All of the biases were scanned to look for sensitivities to particular currents but this did not shed any light on the problem. Typically the measured threshold for a particular channel is quite stable as a function of the bias current in question.

Have also looked for correlations between preamp output DC levels (using the test pixels from 5 chips) and measured thresholds; no such correlation apparent.

These plot illustrate the extent of the the extent of the threshold dispersion. In the upper plot the threshold is shown versus pixel ID for 5 chips (external charge injection).

The pattern varies from chip to chip and is haphazard. For a particular chip however the pattern is repeatable (whether internal or external injection is employed).

In the lower plot a Gaussian fit to the whole distribution yields a sigma of 2326e-.

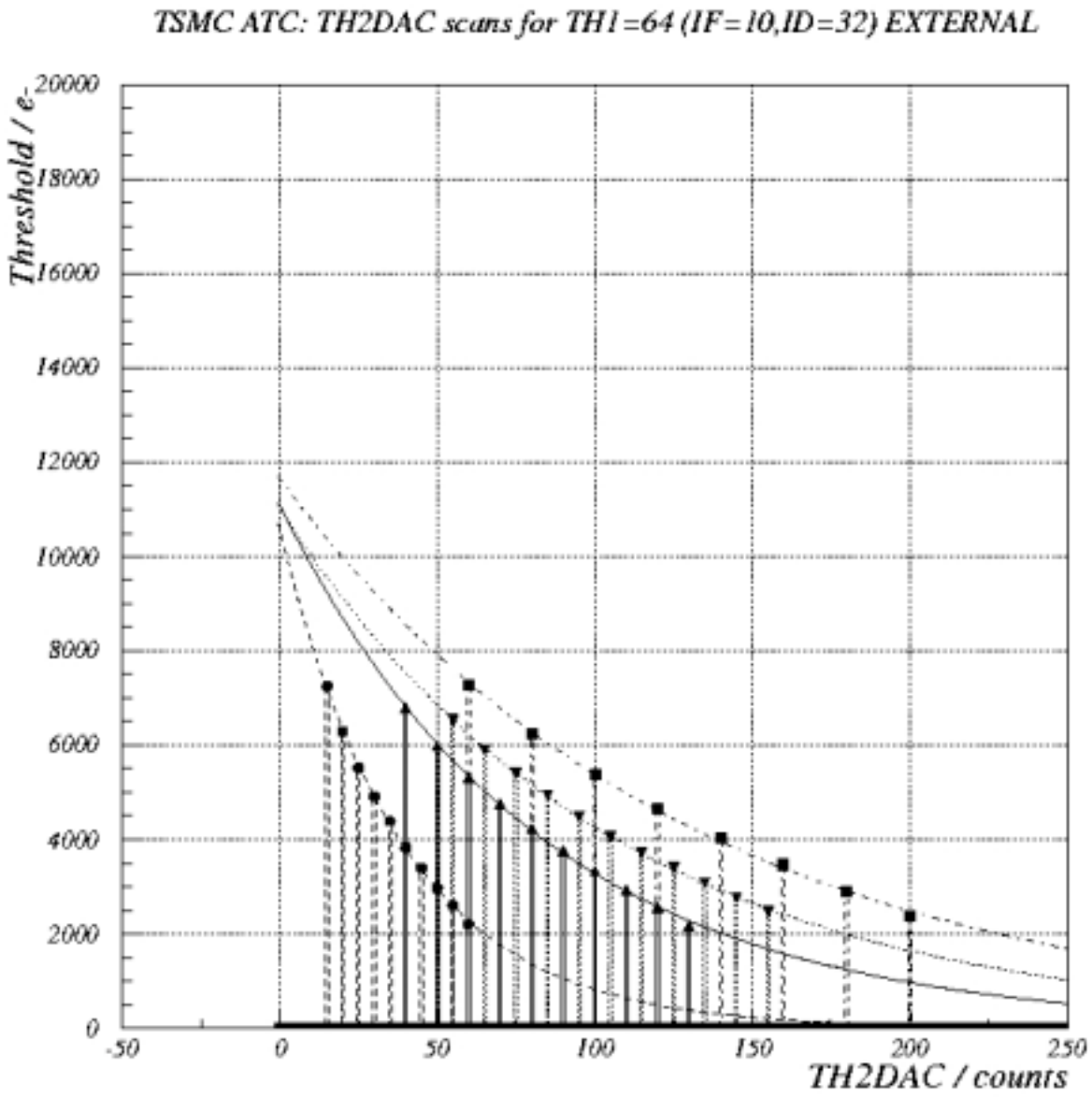


Here for 4 pixels the threshold tuning DAC TH2DAC is varied and the threshold measured.

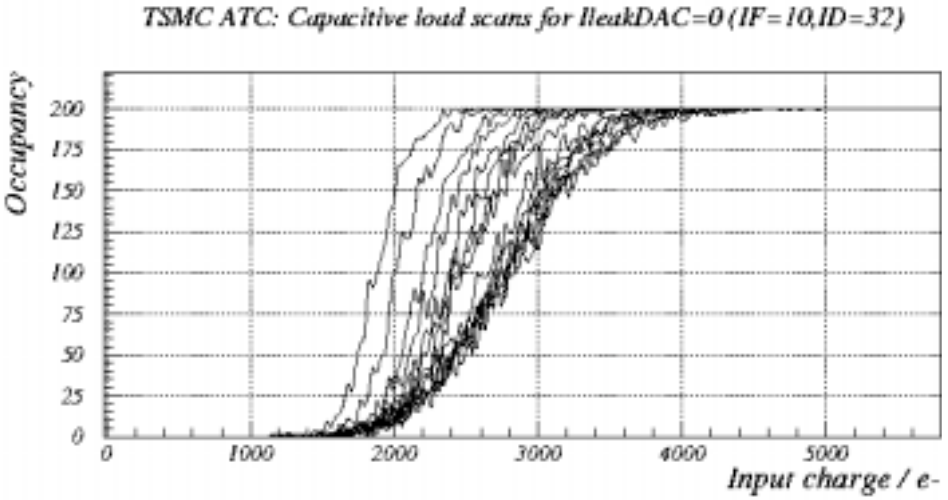
TH1DAC was set to 64.

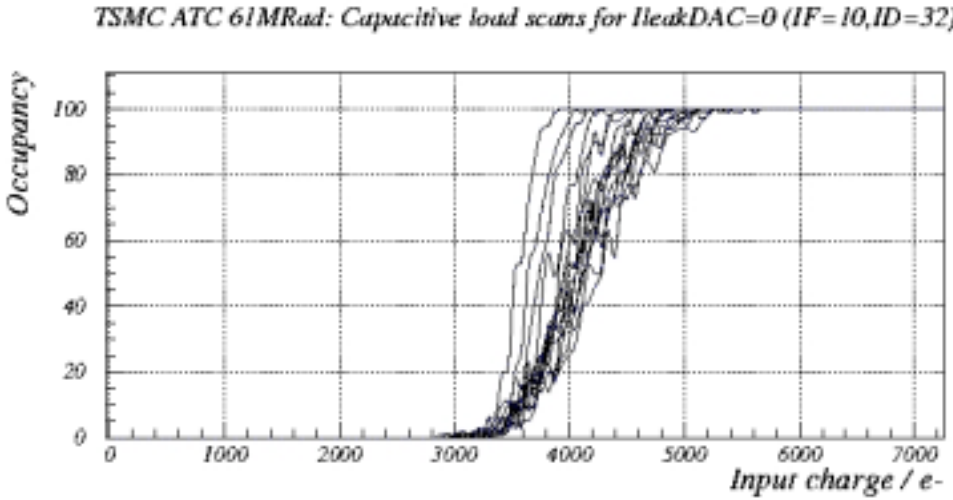
These plots indicate the threshold differences between channels cannot be attributed to pure offsets. Rather it looks more like a gain issue.

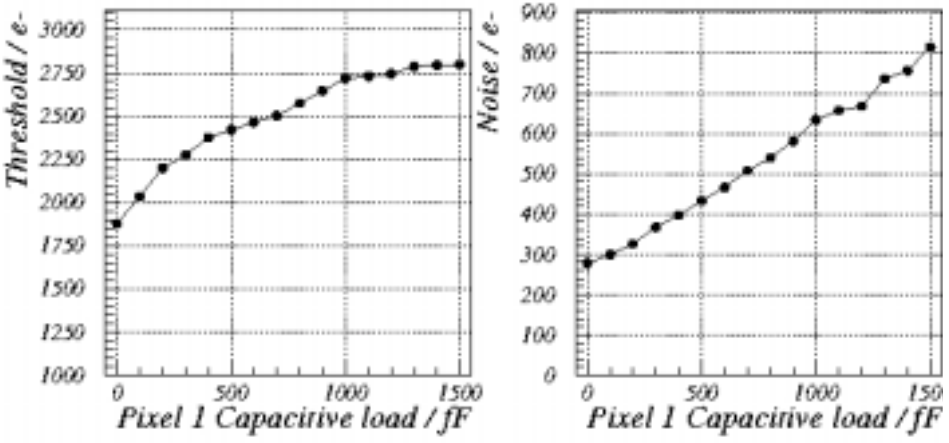
TH2DAC=100 should correspond to a zero threshold but as can be seen in this plot some channels continue to work well beyond this TH2DAC value with large thresholds.

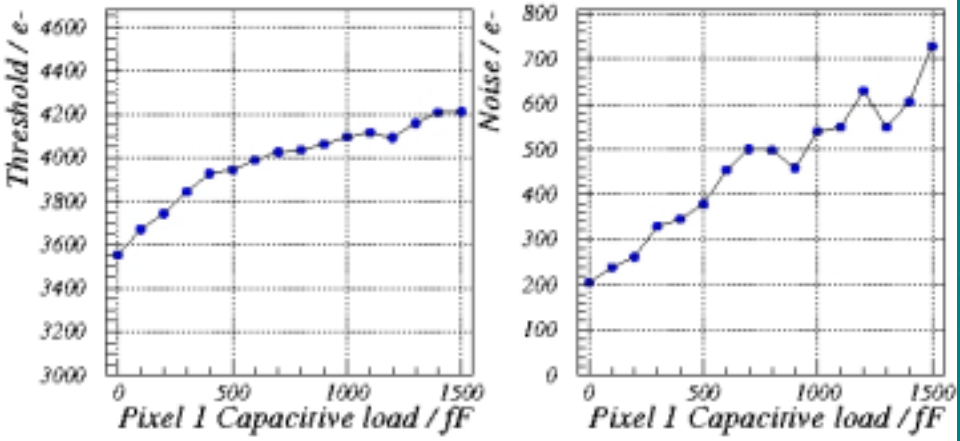


Threshold and noise versus the applied load capacitance measured before and after 61MRad dose with no leakage injection. Capacitance slope is determined to be ~30e-/100fF. We anticipate ~350fF sensor load. The higher noise pre-irrad is due to pickup. A conservatively high enc estimate after irradiatio at 400fF is ~350e-.

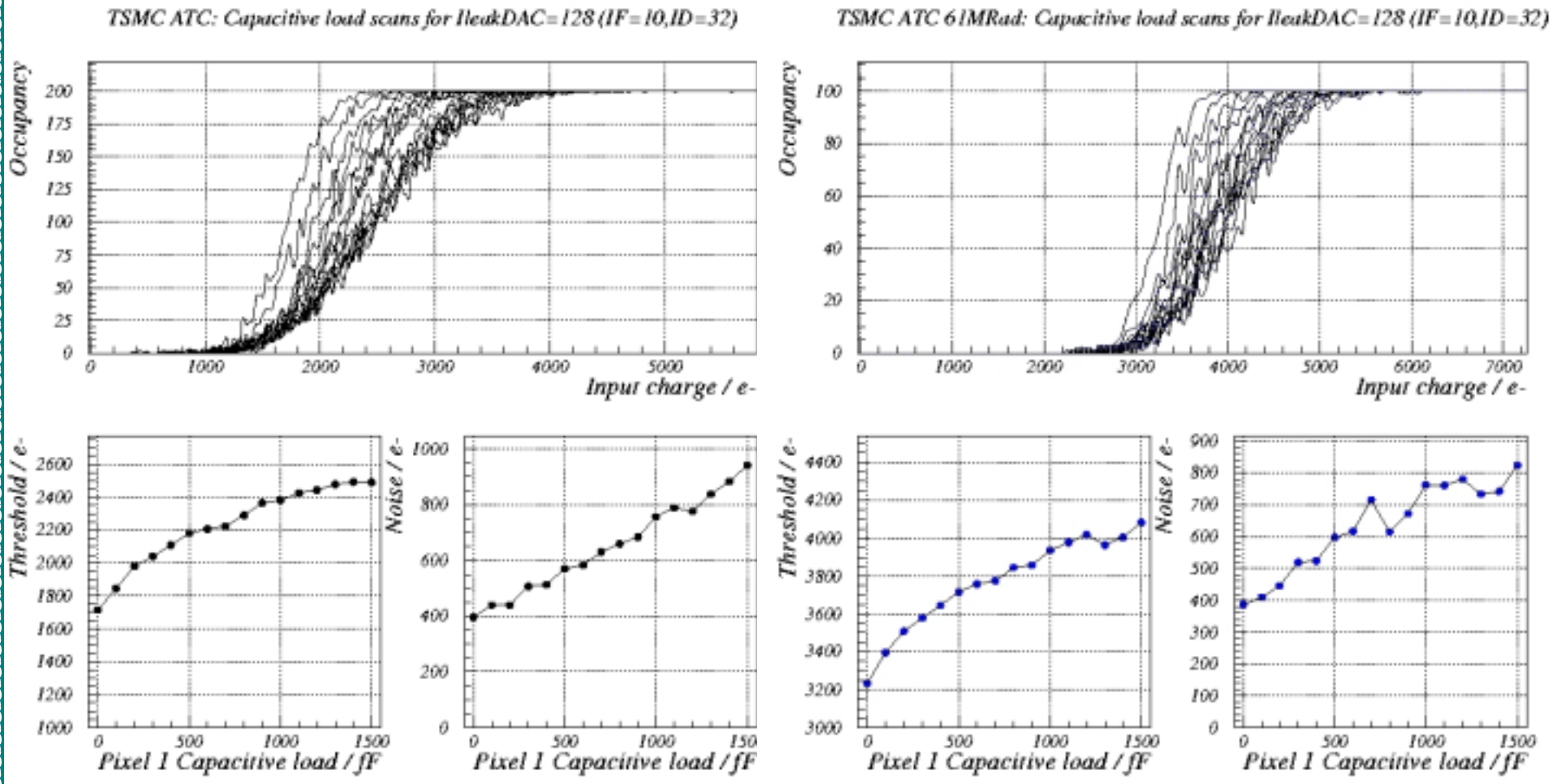






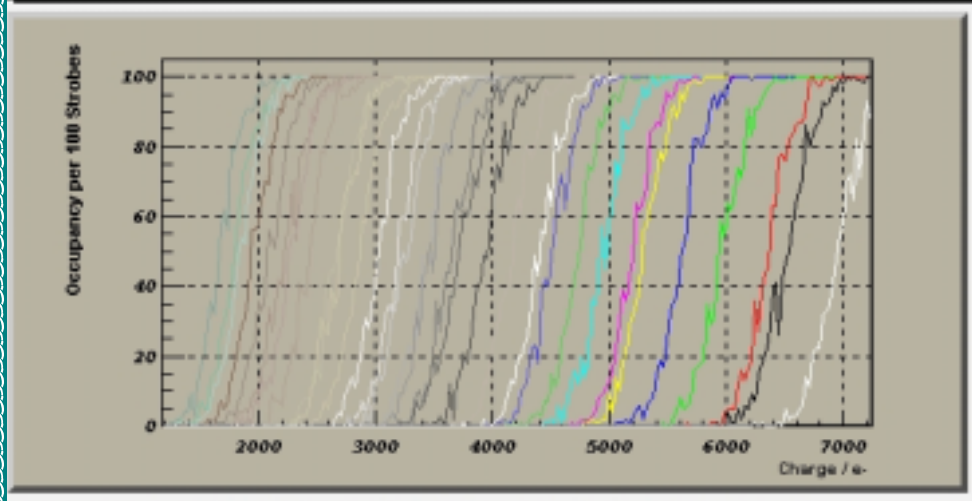


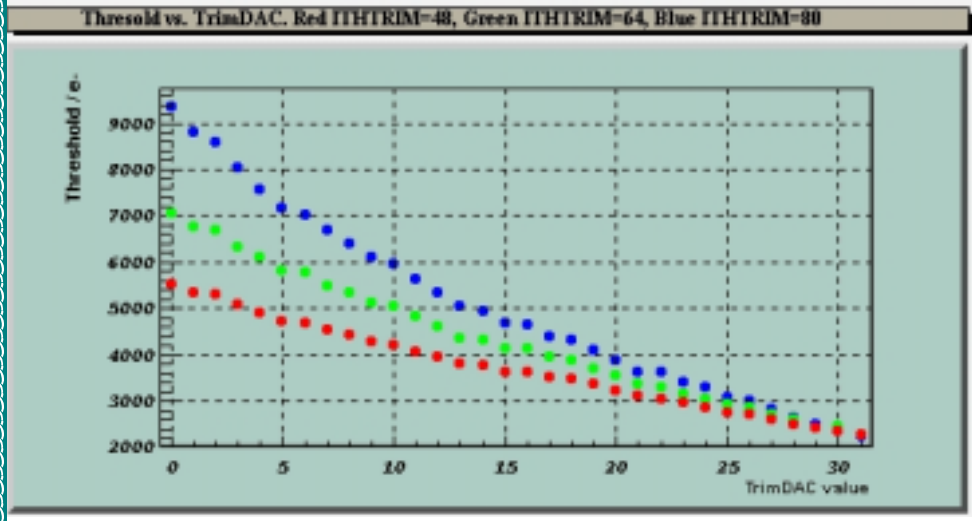
With 50nA injected leakage current the noise figure at 400fF after 60MRad irradiation is around 500e-. A more careful treatment of this measurement is required however to obtain a realistic value.



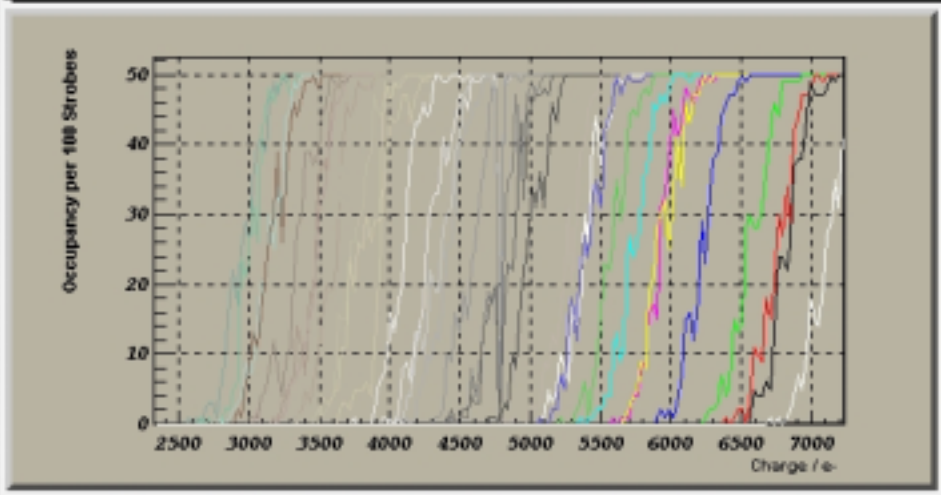
TrimDAC Verification

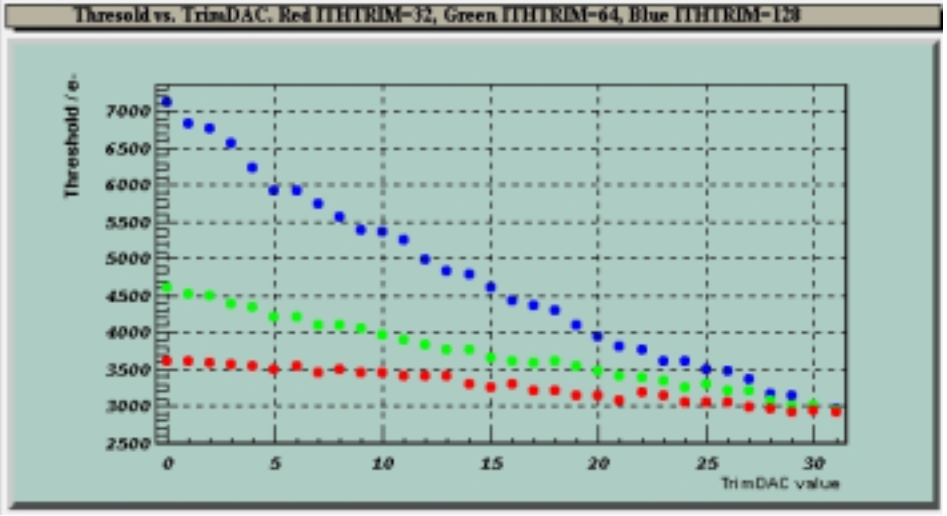
Threshold vs. TrimDAC setting Pre-Irradiation





Threshold vs. TrimDAC setting Post-Irradiation (61MRad)





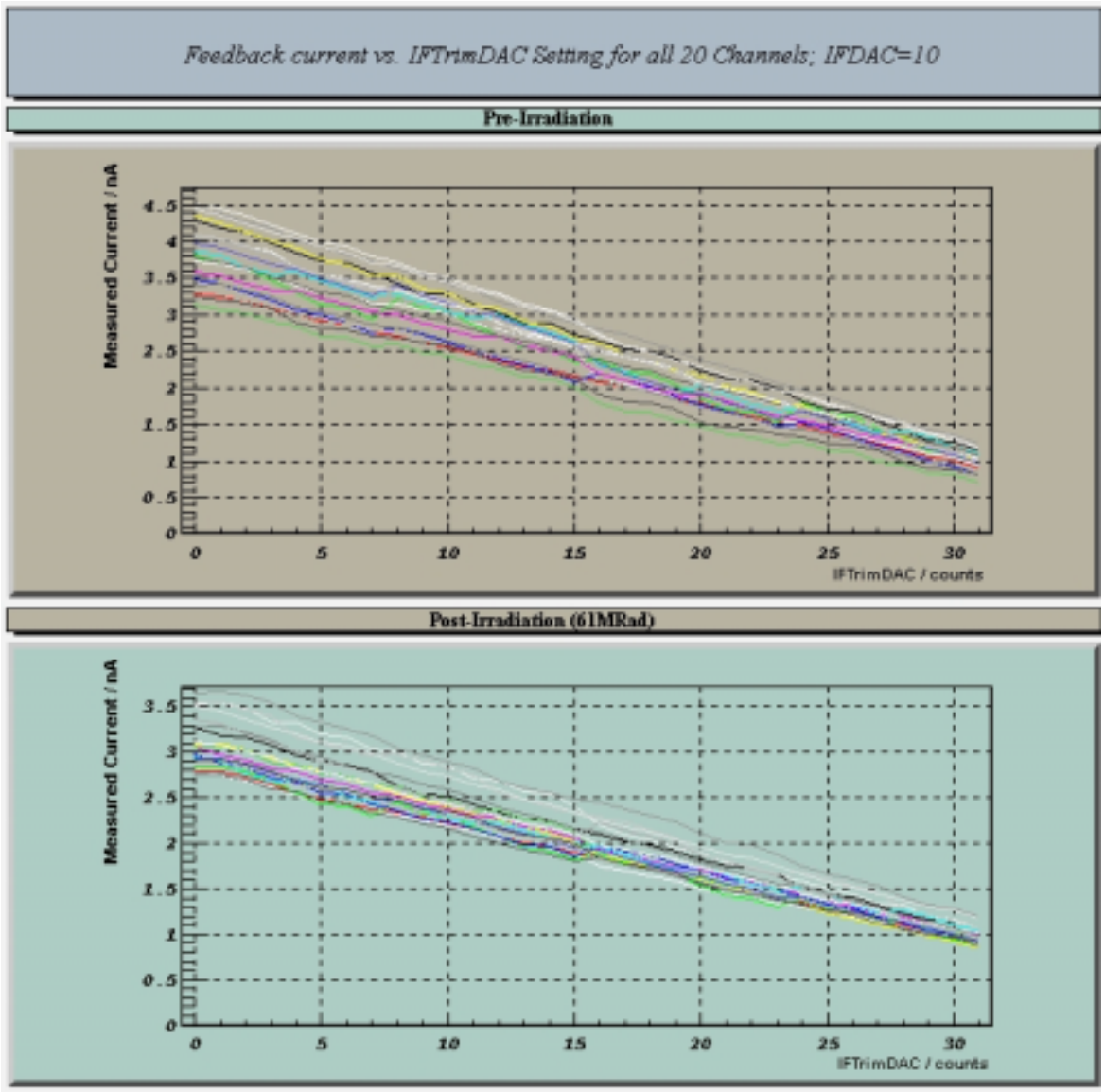
Here the leakage current measurement feature is used to determine very accurately the feedback current.

The upper plot shows the variation of the feedback current for 20 channels as the IFTRIMDAC setting is varied from 0 to 31.

At 31 there is no contribution from IFTRIM and the value corresponds to the bare If value (i.e. from IFDAC), (leakage injection is off).

The dispersion in If and Iftrim is seen to be at the level of +/- 20%.

The lower plot shows the same measurement performed after 61MRad.



LVDS Driver & Receiver

Stand-alone LVDS driver and receiver were incorporated into the analogue test chip.

At 2.0V digital supply voltage, the differential amplitude of the driver was measured to be 360mV (180mV positive and 180mV negative) across 510Ω (~350μA drive current).

At 2.5V the amplitude increases to 190mV –ve and 190mV +ve.

After 60MRad there was no measurable difference in amplitudes.

There does appear to be however a fast spike on the rising edge of the negative output (pre and post irradiation). The simulation indicates the presence of a spike (due to a slightly incorrect implementation of the circuit on the –ve output) but this disappears in the presence of any load capacitance. We observe the spike even with ~10pF of load presented by the scope probe.

The driver circuit operates down to ~1.2V supply.

The LVDS receiver continues to operate down to 50mV input amplitude (with 1.0V offset).

Also the digital supply may be reduced to 1.0V without failure.

The transit time from the differential input (@200mV) to the CMOS output was measured to be ~3ns.

This was a very preliminary study which proved the operation of the circuits. More careful study is required to fully evalute them however.

Test-Pixel Output Buffer

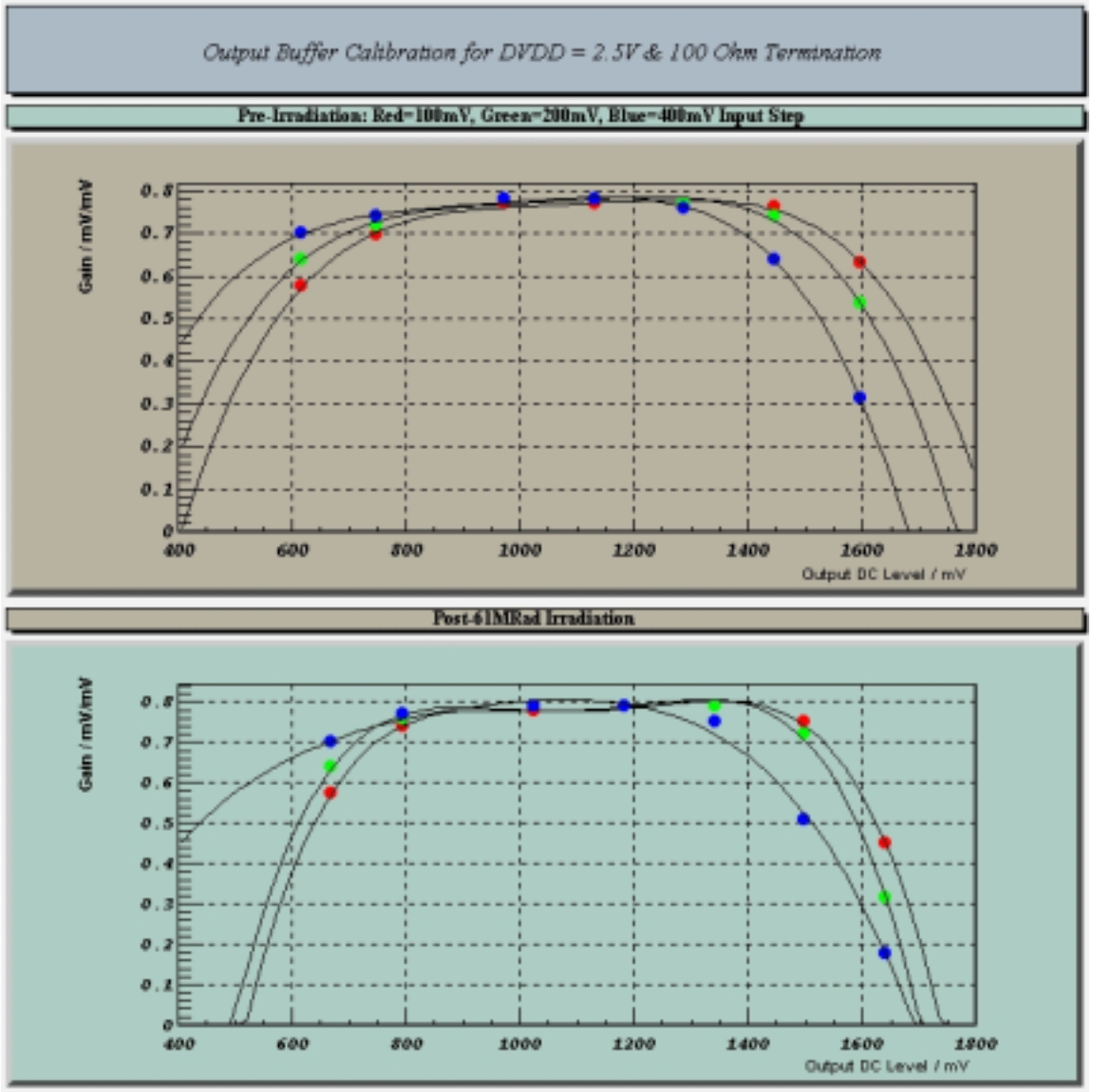
These plots depict the gain of the output buffer over a range of DC offsets on the output.

The red points are for a 100mV input pulse amplitude, green = 200mV and blue = 400mV.

The upper plot is unirradiated and the lower is after 61MRad

In the flat region the gain is very linear within these amplitude values.

The effect of radiation is very minimal. Obtain ~0.79 gain factor at a 1.0V offset for both.



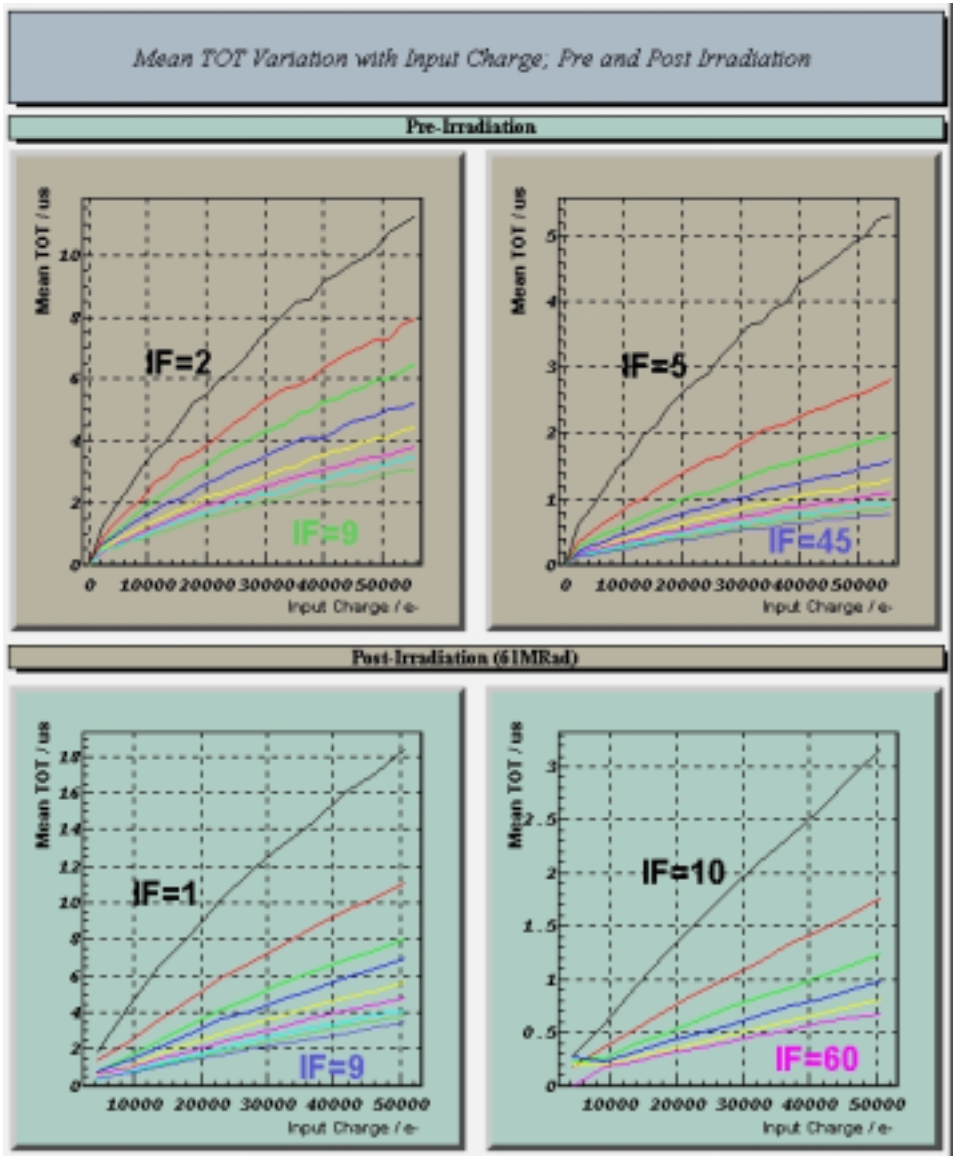
Time-Over-Threshold Performance

These plots show the mean time-over-threshold measured for a range of feedback current values before and after irradiation.

IF = 10 corresponds to 1nA of feedback current.

Setting IFDAC to 10 gives ~1.5us return-to-basline for 1MIP of injected charge.

There is no observable effect from 61MRad dose.



Timewalk Performance

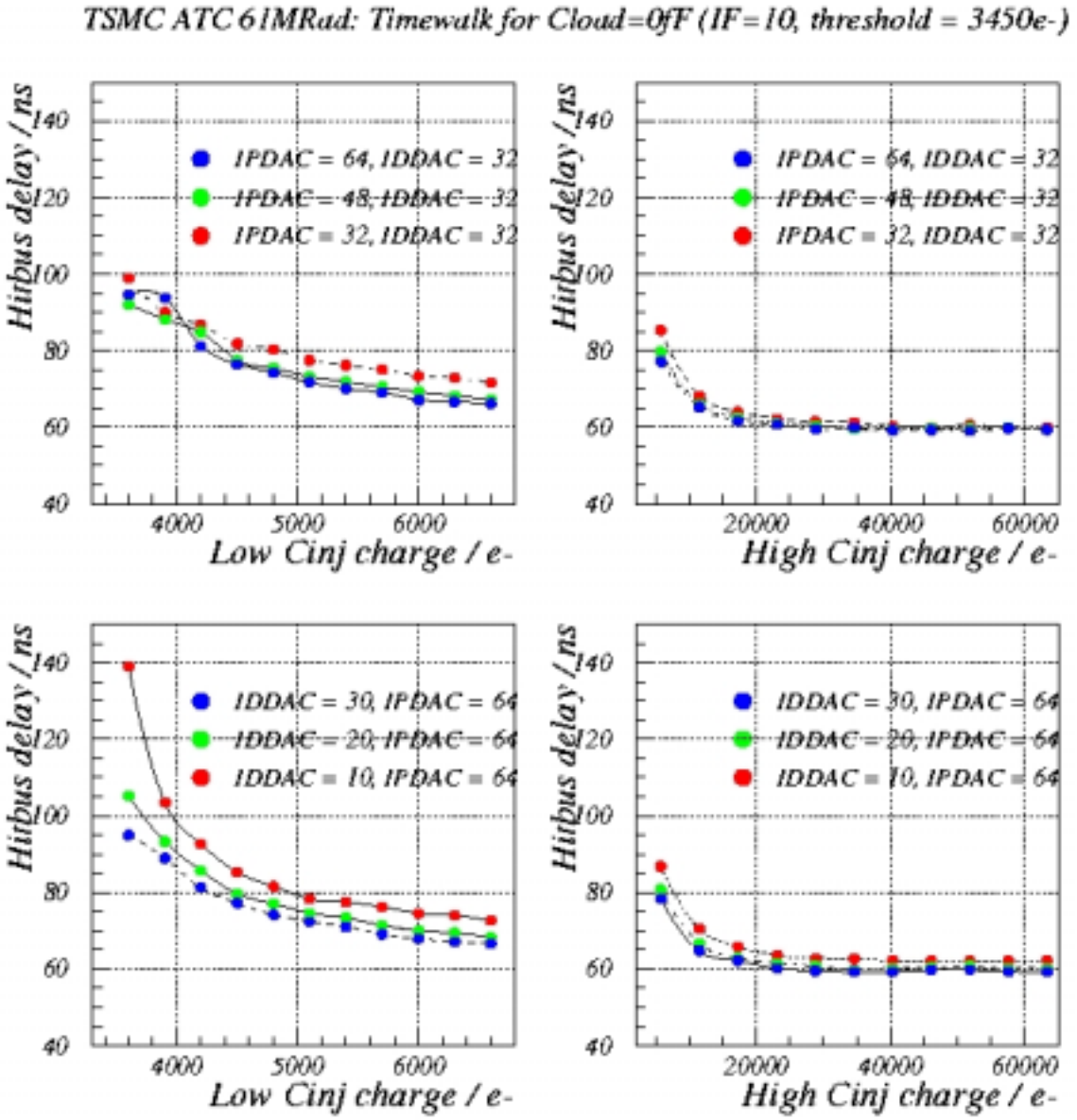
Here the delay between the input pulse and the hitbus signal from the preamp is measured as a function of charge (after 61MRad).

The absolute delay values are meaningless (include cable delays etc.) but differences are relevant.

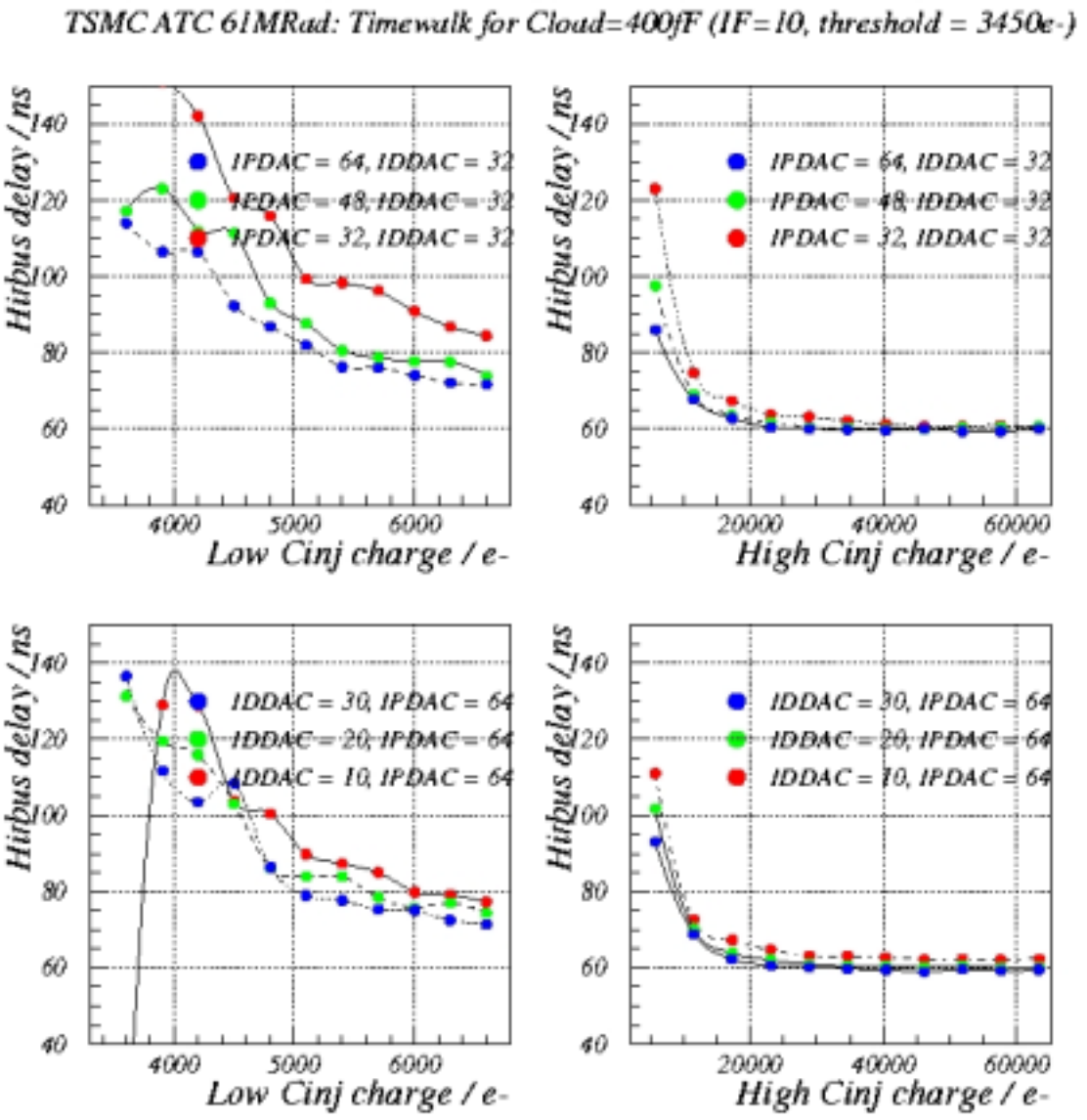
The data in the upper plots is for 3 settings of the preamp bias IPDAC (32,48,64) with IDDAC = 32.

In the lower plots the discriminator bias is varied (10,20 & 30) whilst IPDAC is set to 64.

Without any load capacitance the 20ns timewalk charge is ~600e- over threshold.



Upon application of 400fF of load capacitance, 20ns of timewalk is measured at an input charge of ~1550e- over threshold. This is best case with IPDAC at 64 (8uA) and IDDAC at 32 (2.6uA).

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